8x16 Analog Switch Array Chip CH446Q

5x24 Analog Switch Array Chip CH446X

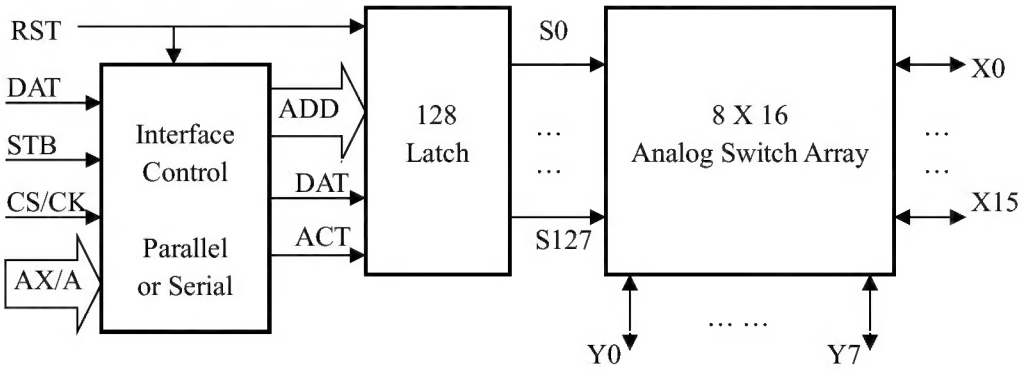
Datasheet

Version: 1D

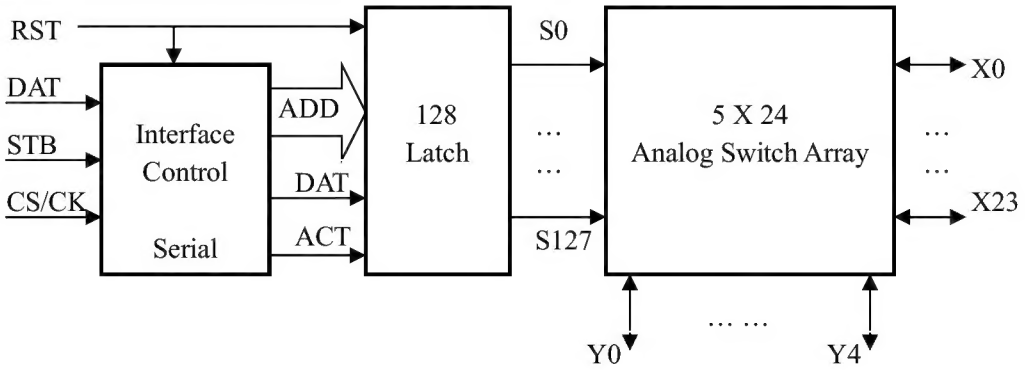
http://wch.cn

1. Overview

CH446Q is an 8x16 matrix analog switch chip. CH446Q contains 128 analog switches, which are distributed at each cross point of 8x16 signal channel matrices. Each analog switch can be turned on or off independently, so as to realize arbitrary routing of 8x16 signal channel.



CH446X is a 5x24 matrix analog switch chip. CH446X contains 120 analog switches, which are distributed at each cross point of 5x24 signal channel matrices. Each analog switch can be turned on or off independently, so as to realize arbitrary routing of 5x24 signal channel.

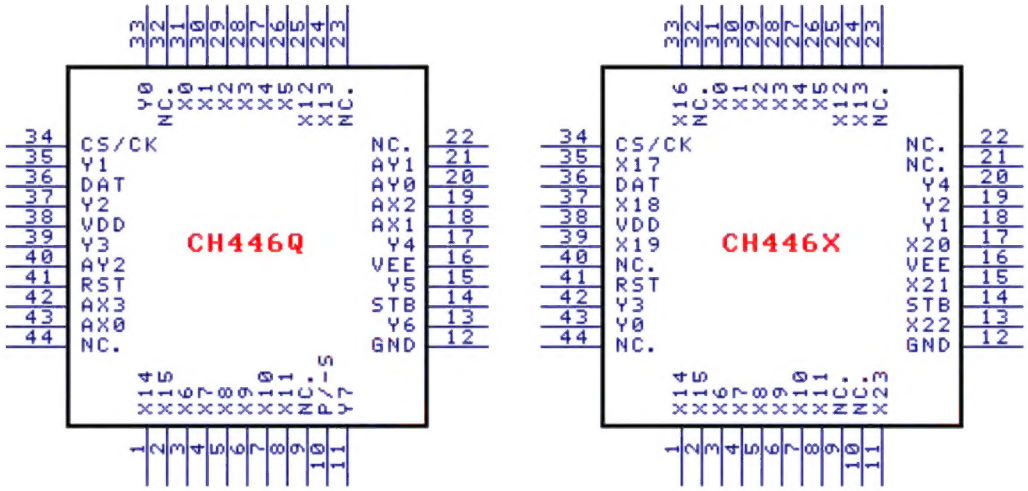


2. Features

- CH446Q has 128 built-in independent analog switches, which are distributed at each cross point of 8x16 signal channel matrices.
- CH446X has 120 built-in independent analog switches, which are distributed at each cross point of 5x24 signal channel matrices.
- CH446Q supports 7-bit parallel address input and is compatible with existing similar products.
- Support serial address shift input to save pins.
- Support 4-12V single supply voltage, support +5V and -7V dual supply voltage.
- When the voltage difference of positive and negative power supply is 12V, the on resistance Ron is 65Ω to the maximum, and △ Ron is not more than 10Ω.
- Pure CMOS process, low static power.

- Adopt LQFP-44 lead-free package, be compatible with RoHS, provide the conversion board for converting into PLCC44 package.

3. Package



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP 44-pin patch	CH446Q
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP 44-pin patch	CH446X

4. Pins

4.1. CH446Q

Pin No.	Pin name	Type	Pin description
38	VDD	Power	Positive power, voltage more than or equal to that of GND
12	GND	Power	Common ground, digital signal reference ground, voltage of 0V
16	VEE	Power	Negative power, voltage less than or equal to that of GND
41	RST	Input	External manual reset input, active at high level
10	P/-S	Input	Address input mode selection: Parallel input mode at high level; serial input mode at low level
36	DAT	Input	Serial data input and switch data input in serial address mode; Switch data input in parallel address mode, On at high level, off at low level
14	STB	Input	Strobe pulse input, active at high level
34	CS/CK	Input	Serial clock input in serial address mode, active on rising edge; Chip selection input in parallel address mode, active at high level

43, 18, 19, 42	AX0～AX3	Input	Unused pins in serial address mode, GND must be directly connected; Port X selected address input in parallel address mode
20, 21, 40	AY0～AY2	Input	Unused pins in serial address mode, GND must be directly connected; Port Y selected address input in parallel address mode
31, 30, 29, 28, 27, 26, 3, 4, 5, 6, 7, 8, 25, 24, 1, 2	X0～X15	Analog signal Input/Output	Port X of 8x16 matrix analog switch
33, 35, 37, 39, 17, 15, 13, 11	Y0～Y7	Analog signal Input/Output	Port Y of 8x16 matrix analog switch
9, 22, 23, 32, 44	NC.	Idle pin	Unused pins. Do not connect

4.2. CH446X

Pin No.	Pin name	Type	Pin description
38	VDD	Power	Positive power, voltage more than or equal to that of GND
12	GND	Power	Common ground, digital signal reference ground, voltage of 0V
16	VEE	Power	Negative power, voltage less than or equal to that of GND
41	RST	Input	External manual reset input, active at high level
36	DAT	Input	Serial data input and switch data input; On at high level, and off at low level when used as switch data input
14	STB	Input	Strobe pulse input, active at high level
34	CS/CK	Input	Serial clock input, active on rising edge
31, 30, 29, 28, 27, 26, 3, 4, 5, 6, 7, 8, 25, 24, 1, 2, 33, 35, 37, 39, 17, 15, 13, 11	X0～X23	Analog signal Input/Output	Port X of 5x24 matrix analog switch
43, 18, 19, 42, 20	Y0～Y4	Analog signal Input/Output	Port Y of 5x24 matrix analog switch
9, 10, 21, 40, 22, 23, 32, 44	NC.	Idle pin	Unused pins. Do not connect

5. Functional Specification

Refer to the block diagram on the home page. CH446Q chip is divided into three parts: interface control logic, 128 latches and 128 analog switch arrays. The interface control logic also includes conversion from serial address to parallel address.

128 analog switches are distributed at each cross point of 8x16 matrixes composed of 16 ports X and 8 ports

Y, so that any port X and any port Y can be on or off as required, even two ports X are respectively conducted to a port Y, realizing indirect conduction between any two ports X or any two ports Y.

128 latches are used to respectively control the on-off of 128 analog switches. 128 latches are addressed as 0 to 127, which are selected after decoding of 7-bit addresses ADDR6-ADDR0. All latches can be cleared to 0 by inputting the high level reset signal from RST pin, causing all analog switches to be off. To turn on or off an analog switch, provide the latch address through 7-bit ADDR, and provide switch data through DAT (1 is on, 0 is off), then generate an ACT activated pulse, write the switch data to the latch designated by the ADDR decoder, and realize the control of the designated analog switch.

The interface control logic is used to generate ADDR address and ACT activated pulse. In the parallel address input mode, pins AX0-AX3 and AY0-AY2 constitute 7-bit address to input ADDR0-ADDR6 from low to high. When the chip selection signal input by CS/CK pin is at high level, the high-level strobe pulse input by STB pin generates ACT activated pulse; when CS/CK pin is at low level, no ACT signal is generated. In the serial address input mode, CS/CK pin inputs clock, inputs ADDR6 and ADDR5 to ADDR1 and ADDR0 (respectively corresponding to AY2 and AY1 to AX1 and AX0) in sequence from DAT pin on each rising edge. CS/CK pin shall provide 7 rising edges to get the 7-bit address, and the high level strobe pulse input by STB pin directly generates ACT activated pulse.

In fact, in the parallel address input mode, ACT signal is "and" of CS/CK pin input and STB pin input; in the serial address input mode, ACT signal is only the input from STB pin. RST reset signal takes precedence over ACT signal. When RST inputs high level, ACT signal will be ignored and all latches will always be reset to 0. When ACT activated pulse is active, DAT pin can dynamically change the input switch data and enable the corresponding analog switch to be on or off in real time, but the input data of DAT pin shall remain stable until the end of ACT signal (i.e., before the falling edge of STB) in order to latch the data properly.

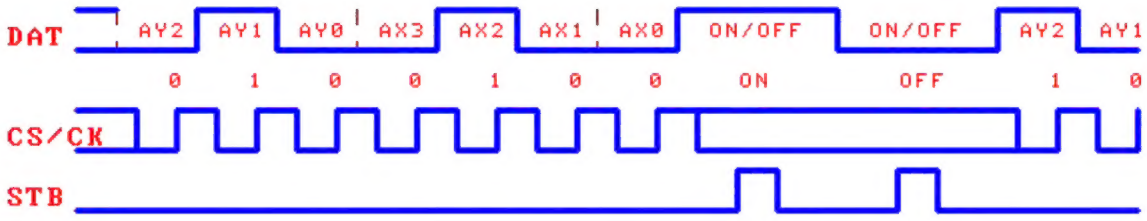
CH446X and CH446Q are similar in function but have three differences: ① . The former has a 5x24 matrix composed of 24 ports X and 5 ports Y, and the latter has an 8X16 matrix composed of 16 ports X ports and 8 ports Y. ② . The former only supports serial address mode, and the latter supports parallel address and serial address mode; ③ . Although CH446X has 128 latches, it has only 120 analog switches, and 8 latches do not have any purpose.

The following table is the decoding truth table of the 7-bit address ADDR for CH446Q chip and the address table of 128 analog switches.

Intersection Point Port Y - Port X	ADDR6 AY2	ADDR5 AY1	ADDR4 AY0	ADDR3 AX3	ADDR2 AX2	ADDR1 AX1	ADDR0 AX0	Address No.
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H
Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH

Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH
Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y1-X0	0	0	1	0	0	0	0	10H
Y1-X1	0	0	1	0	0	0	1	11H
.....								
Y1-X14	0	0	1	1	1	1	0	1EH
Y1-X15	0	0	1	1	1	1	1	1FH
Y2-X0	0	1	0	0	0	0	0	20H
.....								
Y2-X15	0	1	0	1	1	1	1	2FH
.....								
Y7-X0	1	1	1	0	0	0	0	70H
.....								
Y7-X14	1	1	1	1	1	1	0	7EH
Y7-X15	1	1	1	1	1	1	1	7FH

The figure below is an example of a serial address input that controls the analog switch with 24H address (between Y2 and X4), first on and then off.



The following table is the decoding truth table of the 7-bit address ADDR for CH446X chip and the address table of 120 analog switches.

Intersection Point Port Y - Port X	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	Address No.
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H
Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH
Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH

Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y0-X16	0	0	1	0	0	0	0	10H
Y0-X17	0	0	1	0	0	0	1	11H
Y0-X18	0	0	1	0	0	1	0	12H
Y0-X19	0	0	1	0	0	1	1	13H
Y0-X20	0	0	1	0	1	0	0	14H
Y0-X21	0	0	1	0	1	0	1	15H
Y0-X22	0	0	1	0	1	1	0	16H
Y0-X23	0	0	1	0	1	1	1	17H
Y4-X0	0	0	1	1	0	0	0	18H
Y4-X1	0	0	1	1	0	0	1	19H
Y4-X2	0	0	1	1	0	1	0	1AH
Y4-X3	0	0	1	1	0	1	1	1BH
Y4-X4	0	0	1	1	1	0	0	1CH
Y4-X5	0	0	1	1	1	0	1	1DH
No connection	0	0	1	1	1	1	0, 1	1EH, 1FH
Y1-X0	0	1	0	0	0	0	0	20H
.....								
Y1-X23	0	1	1	0	1	1	1	37H
Y4-X6	0	1	1	1	0	0	0	38H
.....								
Y4-X11	0	1	1	1	1	0	1	3DH
No connection	0	1	1	1	1	1	0, 1	3EH, 3FH
Y2-X0	1	0	0	0	0	0	0	40H
.....								
Y2-X23	1	0	1	0	1	1	1	57H
Y4-X12	1	0	1	1	0	0	0	58H
.....								
Y4-X17	1	0	1	1	1	0	1	5DH
No connection	1	0	1	1	1	1	0, 1	5EH, 5FH
Y3-X0	1	1	0	0	0	0	0	60H
.....								
Y3-X23	1	1	1	0	1	1	1	77H
Y4-X18	1	1	1	1	0	0	0	78H
.....								
Y4-X23	1	1	1	1	1	0	1	7DH
No connection	1	1	1	1	1	1	0, 1	7EH, 7FH

6. Parameters

6.1. Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VDD	VDD supply voltage when VEE=GND=0V,	-0.5	16	V
VEE	VEE supply voltage when VDD=GND=0V,	-16	+0.5	V
Vaio	Voltage on analog signal input or output pin, VDD>=GND>=VEE	VEE-0.5	VDD+0.5	V
Vdio	Voltage on digital signal input or output pin, VDD>=GND>=VEE	GND-0.5	VDD+0.5	V
Isw	Continuous through current of analog switch	0	15	mA
Iall	Total continuous through current of all analog switches	0	100	mA

6.2. Recommended Operating Voltage

Name	Parameter description		Min	Max	Unit
VDD	GND=0V，The voltage difference between VDD and VEE is less than 13.2V	VDD supply voltage	4	13.2	V
VEE		VEE supply voltage	-8.8	0	V
Vaio	Voltage on analog signal input or output pin, VDD>=GND>=VEE		VEE	VDD	V
Vdio	Voltage on digital signal input or output pin, VDD>=GND>=VEE		GND	VDD	V

The supply voltage shall meet two conditions: VDD>GND>=VEE and VDD>GND+4V. The following combinations are recommended:

VDD=12V & GND=0V & VEE=0V （VDD-GND=12V，VDD-VEE=12V）
VDD=5V & GND=0V & VEE=0V （VDD-GND=5V，VDD-VEE=5V）
VDD=6V & GND=0V & VEE=-6V （VDD-GND=6V，VDD-VEE=12V）
VDD=5V & GND=0V & VEE=-7V （VDD-GND=5V，VDD-VEE=12V）
VDD=5V & GND=0V & VEE=-5V （VDD-GND=5V，VDD-VEE=10V）

6.3. Electrical Parameters

Test Conditions: TA=25℃, VDD=12V, GND=0V, VEE=0V, voltage difference between two ends of analog switch: 0.4V

Name	Parameter description	Min.	Typ.	Max.	Unit
ICC0	Static supply current, all digital pins connected to VDD or GND		1	100	uA
ICC5	Static supply current, VDD=5V, all digital pins at 2.4V		0.4	1.5	mA
ICC12	Static supply current, all digital pins at 3.4V		5	15	mA
VIL	Low level input voltage of digital pin, VDD-GND=5V	-0.5		0.8	V
VIH	High level input voltage of digital pin, VDD-GND=5V	2.0		VDD+0.5	V
VIH12	High level input voltage of digital pin	3.3		VDD+0.5	V
ILEAK	Input leakage current of digital pin		0.1	10	uA

IOFF	Leakage current of analog switch in off state		±1	±500	nA
RON12	Analog switch on resistance, VDD-VEE=12V, 25°C		45	65	Ω
RON12T	Analog switch on resistance, VDD-VEE=12V, 85°C		55	80	Ω
RON5	Analog switch on resistance, VDD-VEE=5V, 25°C		120	185	Ω
RON5T	Analog switch on resistance, VDD-VEE=5V, 85°C		150	225	Ω
△RON	On resistance difference of multiple analog switches, VDD-VEE=12V		5	10	Ω

6.4. Timing Parameters of Analog Switch

Test Conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, analog signal 2Vpp

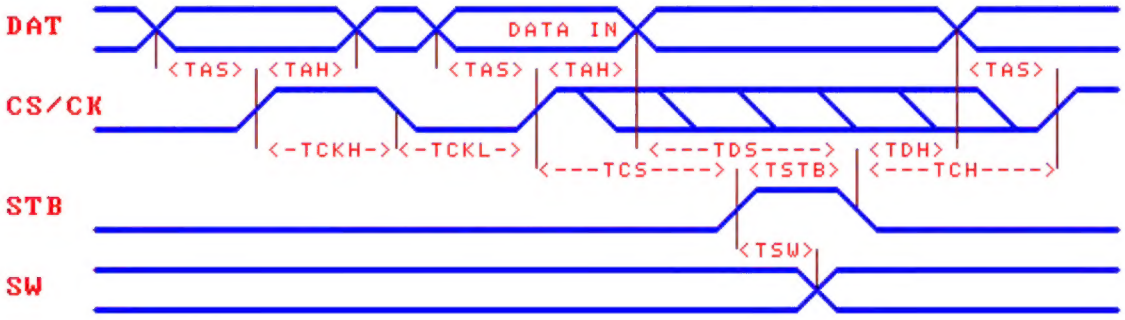
Name	Parameter description	Min	Typ	Max	Unit
CSW	Pin capacitance of analog switch port, F=1MHz		10	25	pF
CFT	Feed-through capacitance of analog switch, F=1MHz		0.5		pF
F3DB	Frequency response of analog switch , 3DB, RL=3KΩ		50		MHz
TPS	Signal-through delay of analog switch , RL=1KΩ, CL=50pF		12	30	nS

6.5. Interface Timing Parameters

Test Conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, refer to the attached figure.

Name	Parameter description	Min.	Typ.	Max.	Unit
CDI	Pin capacitance of digital signal input, F=1MHz		7	15	pF
TPAS	Setup time of parallel input address to STB rising edge	8			nS
TPAH	Hold time of parallel input address to STB falling edge	6			nS
TAS	Setup time of DAT input address to CS/CK rising edge	7			nS
TAH	Hold time of DAT input address to CS/CK rising edge	3			nS
TDS	Setup time of DAT input data to STB falling edge	8			nS
TDH	Hold time of DAT input data to STB falling edge	6			nS
TCS	Setup time of CS/CK rising edge to STB rising edge	10			nS
TCH	Hold time of CS/CK rising edge to STB falling edge	7			nS
TCKL	Low level width of CS/CK clock signal	10			nS
TCKH	High level width of CS/CK clock signal	10			nS

TSTB	Width of STB input active high pulse	10			nS
TRST	Width of RST input active high pulse	15			nS
TSW	Execution delay of DAT, STB or RST to analog switch	5	30	70	nS



7. Applications

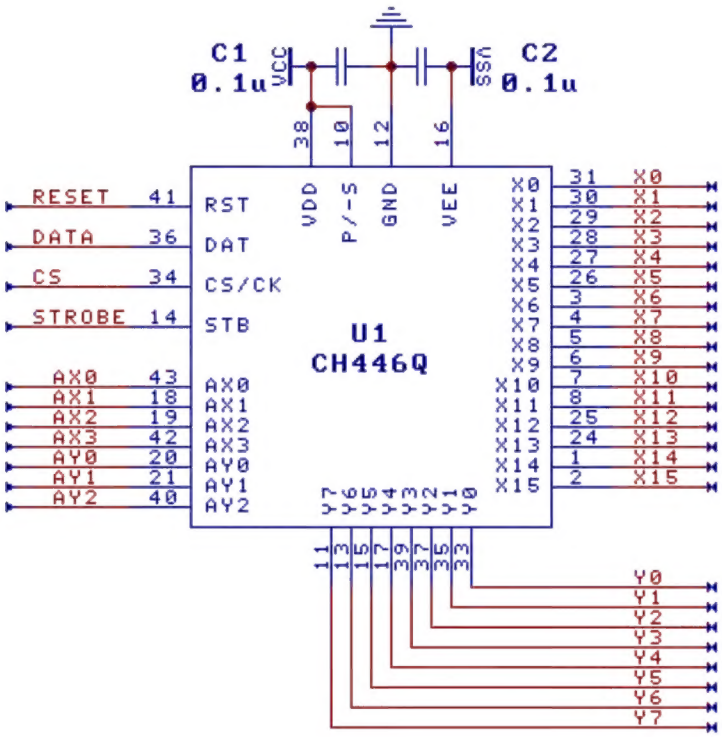
7.1. Parallel Address Input (as shown in figure below)

Control steps in parallel address input mode: provide addresses through pins AX0-AX3 and AY0-AY2 pins, provide data through DAT pin, and provide a high level pulse to STB pin (and CS/CK pin).

In the parallel address input mode, in order to save the control pins of MCU, CS/CK pin can be shorted with STB pin, or shorted with VDD pin, and only STB pin can be reserved and controlled by MCU.

If VEE is connected to the negative voltage, the analog switch can pass through the analog signal with negative voltage; otherwise, if VEE is connected to GND, the analog switch can only pass through the analog signal higher than -0.3V.

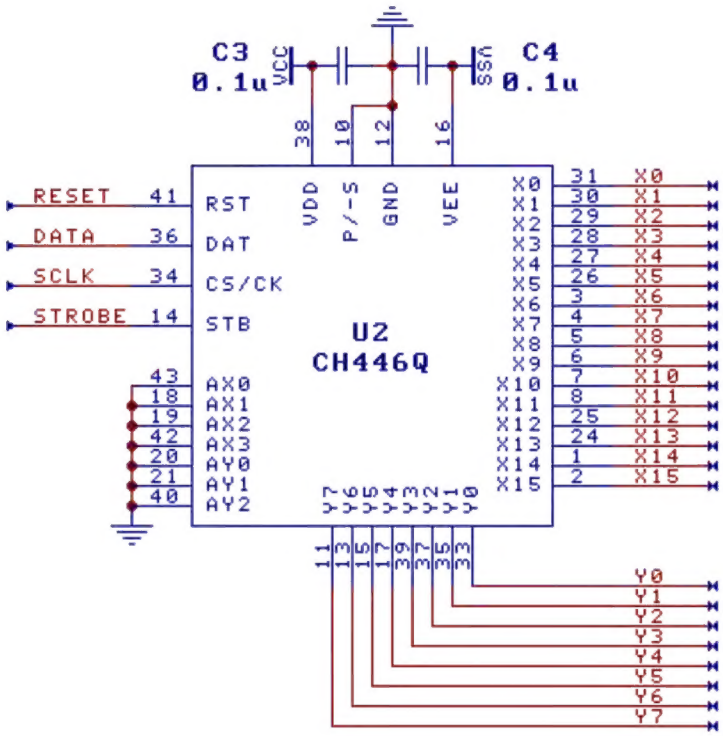
As the analog circuit and the digital circuit share VDD, VDD and VEE pin must be externally connected with the decoupling capacitor to reduce interference. It is recommended to reduce the edge angle of the digital input signal appropriately to reduce transmission frequency. In addition, for the application environment with strong interference, MCU can refresh CH446 every a few seconds to ensure that each analog switch is in the correct on-off state.



7.2. Serial Address Input (Figure below)

Control steps in serial address input mode: provide 7-bit address through DAT pin and move into CH446 by using 7 rising edges of CS/CK pin, provide data through DAT pin, and provide a high level pulse to STB pin.

If MCU is connected with CH446 through SPI bus, the bit 7 of a byte of 8-bit data provided by SPI will be discarded by CH446, the bits 6-0 of SPI will be used as the address, the serial data output pin of SPI for MCU is connected with DAT pin to provide the switch data, and MCU uses an independent pin to control STB pin of CH446.



7.3. MCU Interface Program

The website provides the common C language and ASM assembly interface program for MCU.

7.4. Pin Switching

In the parallel address input mode, CH446Q is basically compatible with MT8816, but the package and the pins are different. The difference is that 8x16 matrix analog switch has part of different pins on port X (or their addresses are different). For the differences, refer to the following table.

ADDR3-ADDR0 or AX3-AX0 addressing	CH446Q packaged with LQFP44		MT8816 packaged with LQFP44	
	Pin No.	Pin name	Pin No.	Pin name
0110	3	X6	31	X12
0111	4	X7	30	X13
1000	5	X8	9	X6
1001	6	X9	10	X7
1010	7	X10	11	X8
1011	8	X11	12	X9

1100	25	X12	13	X10
1101	24	X13	14	X11

The PLCC44 packaged conversion board can realize the conversion from LQFP44 to PLCC44 by adjusting the pin sequence through the internal PCB routing according to the above table.